

1 **CLAIMS**

2 1. A method comprising:
3 creating mappings from a logical address space to physical memory;
4 identifying portions of the logical address space based on usage;
5 modifying the mappings to reduce the number of physical memory devices
6 that are targeted by the mappings; and
7 receiving memory instructions that reference memory in terms of the
8 logical address space.

9
10 2. A method as recited claim 1, wherein the mappings comprise
11 mappings from one or more virtual address spaces to a physical address space.

12
13 3. A memory controller comprising:
14 means for receiving memory instructions that reference memory in terms of
15 a logical address space;
16 means for identifying portions of the logical address space based on usage;
17 and
18 means for mapping the identified portions of the logical address space to
19 physical memory in a manner that reduces the number of physical memory devices
20 referenced by the identified portions of the logical address space.

21
22 4. A memory controller as recited in claim 3, wherein the means for
23 identifying include means for monitoring the memory instructions to determine
24 more frequently used portions of the logical address space.
25

1 5. A memory controller as recited in claim 3, wherein the means for
2 identifying include means for monitoring the memory instructions to determine
3 more recently used portions of the logical address space.

4
5 6. A memory controller as recited in claim 3, wherein the means for
6 identifying include means for receiving notifications regarding logical memory
7 allocations and de-allocations.

8
9 7. A memory controller as recited in claim 3, wherein the means for
10 identifying include means for receiving notifications regarding actual usage of
11 logical memory addresses.

12
13 8. A memory controller as recited in claim 3, wherein the means for
14 identifying action include means for maintaining one or more in-use registers
15 indicating whether corresponding portions physical memory are currently in use.

16
17 9. A memory controller as recited in claim 3, further comprising:
18 means for identifying one or more memory devices that are not referenced
19 by the identified portions of the logical address space; and
20 means for setting said one or more identified memory devices to a reduced
21 power mode.

1 10. A memory controller as recited in claim 3, wherein the means for
2 identifying includes means for monitoring the memory instructions to determine
3 more frequently used portions of the logical address space, the memory controller
4 further comprising:

5 means for identifying one or more memory devices that are not referenced
6 by the identified portions of the logical address space; and

7 means for setting said one or more identified memory devices to a reduced
8 power mode.

9
10 11. A memory controller as recited in claim 3, wherein the means for
11 identifying includes means for monitoring the memory instructions to determine
12 more recently used portions of the logical address space, the memory controller
13 further comprising:

14 means for identifying one or more memory devices that are not referenced
15 by the identified portions of the logical address space; and

16 means for setting said one or more identified memory devices to a reduced
17 power mode.

18
19 12. A memory controller as recited in claim 3, further comprising:
20 means for identifying one or more physical memory areas that are
21 referenced by the identified portions of the logical address space; and

22 means for setting said one or more physical memory areas to a reduced
23 power mode.

1 **13.** A memory controller as recited in claim 3, wherein the means for
2 identifying includes means for monitoring the memory instructions to determine
3 more frequently used portions of the logical address space, the memory controller
4 further comprising:

5 means for identifying one or more physical memory areas that are not
6 referenced by the identified portions of the logical address space; and

7 means for setting said one or more physical memory areas to a reduced
8 power mode.

9
10 **14.** A memory controller as recited in claim 3, wherein the means for
11 identifying includes means for monitoring the memory instructions to determine
12 more recently used portions of the logical address space, the memory controller
13 further comprising:

14 means for identifying one or more physical memory areas that are not
15 referenced by the identified portions of the logical address space; and

16 means for setting said one or more physical memory areas to a reduced
17 power mode.

18
19 **15.** A memory controller as recited in claim 3, further comprising means
20 for periodically repeating the identifying and mapping actions to repeatedly reduce
21 the number of physical memory devices referenced by the identified portions of
22 the logical address space.

1 **16.** A memory controller as recited in claim 3, further comprising:
2 means for periodically repeating the identifying and mapping actions to
3 repeatedly reduce the number of physical memory devices referenced by the
4 identified portions of the logical address space; and

5 means for moving affected portions of physical memory so that each
6 logical address continues to reference the same data prior to any repeated mapping
7 action.

8
9 **17.** A method of managing memory, comprising:
10 monitoring memory accesses to identify portions of a logical address space
11 based on usage; and

12 periodically re-mapping the logical address space to physical memory to
13 reduce the number of physical memory devices referenced by the identified
14 portions of the logical address space.

15
16 **18.** A method as recited in claim 17, wherein the monitoring comprises
17 monitoring the memory instructions to determine more frequently used portions of
18 the logical address space.

19
20 **19.** A method as recited in claim 17, further wherein the monitoring
21 comprises monitoring the memory instructions to determine more recently used
22 portions of the logical address space.

1 **20.** A method as recited in claim 17, further comprising:
2 receiving memory instructions that reference memory in terms of the
3 logical address space; and
4 monitoring the memory instructions to identify the portions of the logical
5 address space.

6
7 **21.** A method as recited in claim 17, wherein the identified portions of
8 the logical address space are those portions that are used least frequently, further
9 comprising:

10 identifying one or more memory devices that are not referenced by the
11 identified portions of the logical address space; and

12 setting said one or more identified memory devices to a reduced power
13 mode.

14
15 **22.** A method as recited in claim 17, wherein the identified portions of
16 the logical address space are those portions that are used least recently, further
17 comprising:

18 identifying one or more memory devices that are not referenced by the
19 identified portions of the logical address space; and

20 setting said one or more identified memory devices to a reduced power
21 mode.

1 **23.** A method as recited in claim 17, wherein the identified portions of
2 the logical address space are those portions that are used least frequently, further
3 comprising:

4 identifying one or more physical memory areas that are not referenced by
5 the identified portions of the logical address space; and

6 setting said one or more physical memory areas to a reduced power mode.

7
8 **24.** A method as recited in claim 17, wherein the identified portions of
9 the logical address space are those portions that are used least recently, further
10 comprising:

11 identifying one or more physical memory areas that are not referenced by
12 the identified portions of the logical address space; and

13 setting said one or more physical memory areas to a reduced power mode.

14
15 **25.** A method as recited in claim 17, further comprising:

16 prior to any re-mapping action, moving affected portions of physical
17 memory so that each logical address continues to reference the same data.

18
19 **26.** A system comprising:

20 a plurality of physical memory devices containing physical memory;

21 a memory controller configured to reference the physical memory in
22 response to received memory instructions specifying addresses in terms of a
23 logical address space;

1 an operating system configured to dynamically allocate memory from the
2 logical address space and to identify allocated portions of the logical address space
3 to the memory controller;

4 wherein the memory controller is configured to respond to the operating
5 system by mapping allocated portions of the logical address space to
6 corresponding portions of physical memory in a manner that tends to reduce the
7 number of physical memory devices referenced by the allocated portions of the
8 logical address space.

9
10 **27.** A system as recited in claim 26, wherein:

11 the operating system is further configured to dynamically de-allocate
12 memory from the logical address space and to identify the de-allocated portions of
13 the logical address space to the memory controller; and

14 the memory controller is further configured to respond to identifications of
15 de-allocated portions of the logical address space by re-mapping currently
16 allocated portions of logical memory to reduce the number of physical memory
17 devices referenced by allocated portions of logical memory.

18
19 **28.** A system as recited in claim 26, wherein the memory controller is
20 configured to maintain one or more in-use registers indicating which portions of
21 physical memory are currently in use.

22
23 **29.** A memory management system comprising:

24 means for maintaining a free region list indicating free memory regions for
25 potential allocation from physical memory devices;

1 means for sorting the free region list in an order that is based on the relative
2 current allocations of memory regions from respective sets of one or more
3 physical memory devices; and

4 means for allocating memory regions indicated by the sorted free region list
5 on the sorted order so that the memory regions are allocated preferentially from
6 those physical memory devices having higher relative current allocations of
7 memory regions.

8
9 **30.** A memory management system as recited in claim 29, further
10 comprising:

11 means for identifying one or more memory devices having relatively lower
12 current allocations of memory regions; and

13 means for setting said one or more identified physical memory devices to a
14 reduced power mode.

15
16 **31.** A memory management system as recited in claim 29, further
17 comprising means for maintaining the free region list as a linked list of free region
18 indicators.

19
20 **32.** A memory management system as recited in claim 29, further
21 comprising means for repeatedly re-sorting the free region list in said order.
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